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PTo/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
JRL-550-509	

Application Number	Filed
10/781,883	February 20, 2004
First Named Inventor: SEAL	
Art Unit: 2183	Examiner: Fennema

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

February 21, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEAL, D. et al.

Atty. Ref.: 550-509; Confirmation No. 1688

Appl. No. 10/781,883

TC/A.U. 2183

Filed: February 20, 2004

Examiner: Fennema

For: INSTRUCTION ENCODING WITHIN A DATA PROCESSING APPARATUS HAVING MULTIPLE INSTRUCTION SETS

* * * * * * * * * * * *

February 21, 2008

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1-6, 8-17, 19-28, and 30-33 stand rejected as being anticipated by Qureshi et al. (2004/00308856). This rejection is in error.

The technology in this case relates to a data processing system having multiple instruction sets and the way in which such multiple instruction sets may be encoded. A data processing system supporting multiple instruction sets allows considerable flexibility in the way in which program operations may be represented, and that flexibility can yield improved code density. But the typical trade-off is increased hardware to support the multiple instruction sets. The inventors overcame this problem by arranging the encoding of the instruction sets such that a common subset of instructions has the same encoding, after variations due to storage order, e.g. endianness, have been compensated for. As a result, the data processing system implementation can be advantageously simplified by using a common decoding logic which reduces the hardware needed.

The Examiner admits that Qureshi fails to teach every claimed feature, and so, on its face the anticipation rejection is suspect. The Advisory action states: "Examiner will conceed [sic] that the Applicant is correct in this regard [that the address decode logic of Qureshi does not properly map onto the claimed limitation of a decoder configured to decode program instructions] and that the address decode logic that the Examiner mapped to does not decode program instructions." The Examiner "still asserts that there is a decode which does this in Qureshi, as the limitations of the claim require that the instruction decoder decode program instructions, and can be operable in both modes as disclosed. Therefore, if Qureshi does perform the rest of the claimed invention, Examiner believes it is a fair assertion to say that Qureshi has this decoder."

While one might infer that Qureshi's CPU 401 in Figure 4 includes an decoder of some sort, there is no evidence in Qureshi that such a decoder is what is claimed. The instruction decoder in claim 1 is "operable in a first mode in which program instructions of a first instruction set are decoded and in a second mode in which program instructions of a second instruction set are decoded." Qureshi does not describe a decoder or any other feature that operates in both claimed modes. Instead, Qureshi either stores data in little endian mode or in big endian mode. But storing data in one format or another format has nothing to do with decoder modes in which program instructions of either a first instruction set or a second instruction set are decoded by the same decoder.

The Examiner contends that the claimed first mode is equivalent to the big endian mode of Qureshi, and the claimed second mode is equivalent to the little endian mode of Qureshi. But the big endian and little endian modes are simply different ways of storing data in a register. For example, in Tables 1 and 2 of Qureshi, the same piece of data ABCD059E is shown stored in big endian mode and in little endian mode. Qureshi does not identify this data as a program

instruction. But even if the data of Qureshi was said to be a program instruction, it would be the same instruction whether it is stored in big endian or little endian mode. The Examiner does not refute this in the advisory action. Because Qureshi's instructions stored in the big endian and little endian modes are the same instruction, an instruction stored in the big endian mode would be from the same instruction set as the instruction stored in the little endian mode. Thus, the two modes that the Examiner suggests exist in Qureshi are not modes in which program instructions from two different instruction sets are decoded.

In the second paragraph of the advisory action, the Examiner argues "that the two subsets claimed are not necessarily different subsets, because unless the two are claimed as distinct, there is no requirement to read them as the same subset." Although this sentence is difficult to understand, the Examiner seems to be suggesting that the first and second subsets are the same subset. First, the Examiner's suggestion is an admission that Qureshi does not teach the claimed first and second instruction sets or the first and second respective subsets of these instruction sets. Second, the Examiner is not entitled to adopt an unreasonable interpretation of the claims. The plain meaning of the terms "first" and "second" is to distinguish between multiple, distinct features. A person of ordinary skill in the art would understand that the terms "first instruction set" and "second instruction set" refer to two distinct instruction sets; it is unreasonable and contrived to say otherwise. Third, the Examiner's interpretation must also be consistent with the meaning of the claim terms as understood in light of the specification. The specification plainly contradicts the Examiner's interpretation.

Qureshi also does not disclose "a subset of program instructions of said first instruction set having a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for

storage order differences, all bits are identical." Because Qureshi only describes rearranging the order of storage for a single piece of data, it cannot disclose a subset of program instructions.

In the fourth paragraph of the advisory action, the Examiner states that "in the claimed invention, when saying that you have two instruction sets, and when compensating for their storage differences, are identical in every way, and perform the exact same operation." But this mischaracterizes what is claimed. In the independent claims, a subset of program instructions of the first instruction set has a common storage order compensated encoding with a subset of program instructions of the second instruction set. Thus, the claimed first and second subsets of instructions from their respective instruction sets are such that after compensating for storage differences, all bits are identical. Qureshi does not describe any subset of program instructions—let alone the claimed first and second subsets.

The Examiner argues in the third paragraph of the advisory action that "a subset is a term which can encompass all, none, or part of a set, thus in Qureshi's case, the subset of instructions... is the entire set." But if every instruction in the first and second instruction sets was part of the common subset of program instructions, then the first and second instruction sets would be the same instruction set. If all the instructions are from the same instruction set, then there is only one instruction set. This "only one instruction set" interpretation renders the claim language meaningless, and thus, cannot be the correct interpretation. There would be no need for an instruction decoder that is "operable in a first mode in which program instructions of a first instruction set are decoded and in a second mode in which program instructions of a second instruction set are decoded" if all the all the instructions are from the same instruction set. Thus, Qureshi does not disclose the claimed common subset of instructions formed by a subset of program instructions from the first instruction set and the subset of program instructions from the second instruction set.

Applicants again emphasize that the claimed decoder is not disclosed in Qureshi, as the Examiner rightly admits. The only option left to the Examiner is to demonstrate that the claimed decoder is inherent in Qureshi. The Federal Circuit requires that "extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill'...'Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 49 USPQ 2d 1949, 1950-51 (Fed. Cir. 1999). That extrinsic evidence is missing here. Instead, the Examiner resorts to unreasonable interpretations that rob the independent claim language of its meaning and that highlight the flawed nature of the rejection.

Given the clear errors noted above, the final rejection should be withdrawn and the application passed to allowance.

Respectfully submitted,

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